Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.An automatic threshold voltage control circuit, comprising:
a first capacitor, having a first terminal and a second terminal, wherein said first terminal is coupled to a first voltage level;
a clock generator, for generating a plurality of clock signals; and
a switching capacitor network, coupled to said second terminal of said first capacitor, wherein the switching capacitor network receives an analog signal and said clock signals, stores a portion of charges of said analog signal, and outputs said portion of charges according to said clock signals, and generates a threshold voltage associated with said first capacitor.

[c2] 2.The circuit of claim 1, wherein said switching capacitor network comprises:
a plurality of sensor control switches, wherein one of said sensor control switches is controlled by said clock signals for turning on/off, said sensor control switches are series-connected to for a series structure having a first terminal and a second terminal, said first terminal of

said series structure receiving said analog signal and said second terminal of series structure being coupled to said second terminal of said first capacitor to output said threshold voltage; and

at least a second capacitor, having a first terminal and a second terminal, wherein said first terminal of said second capacitor is coupled to a node connected to two adjacent sensor control switches in said series structure, said second terminal of said second capacitor is coupled to a second voltage level.

[c3] 3.The circuit of claim 2, wherein said of clock signals have a same frequency with different phases respectively.

[c4] 4.The circuit of claim 3, wherein said plurality of clock signals do not overlap.

[c5] 5. The circuit of claim 4, wherein said plurality of sensor control switches are MOSFETs.

[c6] 6.The circuit of claim 5, wherein said first voltage level and said second voltage level are DC voltage levels.

[c7] 7.The circuit of claim 1, wherein said circuit applies to a frequency-shift keying communication system.

[c8] 8.The circuit of claim 1, wherein said circuit applies to an

amplitude-shift keying communication system.

[c9] 9.The circuit of claim 1, wherein said circuit applies to an on/off keying communication system.

[c10] 10.An analog-to-digital signal converter circuit, comprising:

a first capacitor, having a first terminal and a second terminal, wherein said first terminal is coupled to a first voltage level;

a clock generator, for generating a plurality of clock signals;

a switching capacitor network, coupled to said second terminal of said first capacitor, wherein the switching capacitor network receives an analog signal and said clock signals, said switching capacitor network stores a portion of charges of said analog signal, and outputs said portion of charges according to said clock signals, and generates a threshold voltage associated with said first capacitor; and

a comparator, for comparing said threshold voltage with said analog signal and outputting a digital signal.

[c11] 11.The circuit of claim 10, wherein said switching capacitor network comprises:

a plurality of sensor control switches, wherein one of said sensor control switches is controlled by said clock

signals for turning on/off, said sensor control switches are series-connected to form a series structure having a first terminal and a second terminal, said first terminal of said series structure receiving said analog signal and said second terminal of series structure being coupled to said second terminal of said first capacitor so as to output said threshold voltage; and

at least a second capacitor, having a first terminal and a second terminal, said first terminal of said second capacitor being coupled to a connection between two adjacent sensor control switches in said series structure, said second terminal of said second capacitor being coupled to a second voltage level.

[c12] 12.The circuit of claim 11, wherein said of clock signals have a same frequency with different phases respectively.

[c13] 13.The circuit of claim 12, wherein said clock signals do not overlap.

[c14] 14.The circuit of claim 13, wherein said sensor control switches are MOSFETs.

[c15] 15.The circuit of claim 14, wherein said first voltage level and said second voltage level are DC voltage levels.

[c16] 16.The circuit of claim 10, wherein said circuit applies to

a frequency-shift keying communication system.

[c17] 17.The circuit of claim 10, wherein said circuit applies to an amplitude-shift keying communication system.

[c18] 18.The circuit of claim 10, wherein said circuit applies to an on/off keying communication system.

[c19] 19.A method for converter an analog signal to a digital signal, comprising:
providing a first capacitor and a plurality of clock signals;
storing a portion of charges of an analog signal according to said clock signals;
generating a threshold voltage according to said clock signals based on said portion of charges associated with said first capacitor ; and
comparing said threshold voltage with said analog signal in order to output a digital signal.

[c20] 20.The method for converter of claim 19, wherein said clock signals comprises a first clock signal and a second clock signal, said first and second clock signals have a same frequency but not overlapping, and said step of generating said threshold voltage further comprising:
providing a second capacitor;
conducting said analog signal to said second capacitor

according to said first clock signal to store said portion of charges of said analog signal in said second capacitor; and

conducting said first capacitor and said second capacitor in response to said second clock signal in order to generate said threshold voltage based on said portion of charges of said analog signal associated with said first capacitor.